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09/483,712	01/14/2000	Tongbi Jiang	3815US (98-0670)	8743

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EXAMINER
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 21

Application Number: 09/483,712
Filing Date: January 14, 2000
Appellant(s): JIANG ET AL.

Greg T. Warder
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 27, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-20 stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,147,413	Farnworth	11-2000
5,894,107	Lee et al.	4-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth (US 6,147,413) in view of Lee et al. (US 5,894,107).

Farnworth shows (Fig. 2h) a chip scale package comprising a semiconductor die (1004) having an active surface and a plurality of bond pads (1002). The lower surface of a dielectric element (1006) is attached to a portion of the active surface of the die. The lower surface of a plurality of conductive traces (1016) is attached to the upper surface of the dielectric element. Conductive bond members connect each conductive trace to the bond pads. Carrier bonds (1032) are disposed on an upper surface of the conductive trace. An encapsulating material (1018) is disposed on portions of the die, the dielectric element, the conductive traces, the bond members and a portion of the carrier bond. The dielectric element may be any adhesive including polyamide tape or films (col. 4, lines 1-48). The conductive traces may comprise lead fingers or conductive metal. The conductive bond members may comprise any conventional connecting members including metal, wires, aluminum, TAB or thermocompression bonds. The carrier bond comprises conduct metal or solder balls. The encapsulating material is a non-conductive material with a low elastic modulus film such as polyamide. The carrier bond has lower portion that is attached to the upper surface of the conductive trace and the encapsulating material is disposed about the lower portion of the carrier bond. Farnworth shows all of the elements of the claims except the discrete conductive bond connecting the conductive trace to the bond pad. Lee et al. shows (fig. 1) a chip-size package in which a conductive trace (76) is spaced from a bond pad. A discrete conductive bond (80) in the form of a wire connects the conductive trace to a bond pad (74) formed on the surface of a semiconductor chip (72). The trace, discrete bond, and chip are encapsulated by epoxy mold (82). This configuration is a lead on

chip (LOC) which is a specific type of chip-size package. Chip sized package configurations provide the advantage of smaller packages, better electrical performance, higher package density (col. 1, lines 38-51). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conductive trace configuration of Farnworth by employing a lead on chip configuration as taught by Lee to increase the package density and provide better electrical performance.

(11) Response to Argument

The appellants primarily assert that the cited references of Farnworth and Lee et al. cannot be combined because adding the discrete electrical bonds (lead wires) of Lee would enlarge the package size, decrease electrical performance, and add more complicated processing steps. The appellant additionally summarizes that Farnworth teaches away from the use of such discrete electrical bonds to form repattern traces with reduced masking steps. The examiner contends that the combination of Farnworth and Lee is proper. As stated in arguments throughout prosecution, the use of discrete electrical bonds (lead or bond wires) is notoriously well known in the art. The appellant's own prior art figure 1 illustrates bond wires 240 to electrically connect lead 220 to the active surface of the chip 210. The appellant's arguments are an attempt to circumvent Farnworth which was cited in a previous 102 Rejection. The novelty of the applicant's invention pertains to the carrier bonds 50 and how portions of those carrier bonds extend through package encapsulant 60 (see fig. 4). Patentability of the instant

invention should not be based on "bond wires" because they are so well known in the art and furthermore have been properly disclosed in the above 103 Rejection. However, the appellant has chosen to make bond wires the issue of this appeal and the examiner is must rebut.

As stated in the above rejection, Lee was cited to cure the deficiencies of Farnworth by disclosing at least a discrete conductive bond (bond wire) connecting a conductive trace to a bond pad on the active surface of the die. Lee disclosed motivation for using bond wires by stating that the invention provides chip sized package configurations with the advantage of smaller packages, better electrical performance, and higher package density (col. 1, lines 38-51). The applicant's argument that bond wires, if used by Farnworth would enlarge the package size, increase process steps, and decrease electrical performance is completely speculation because Farnworth does not mention anything concerning bond wires used for connection. In fact, Farnworth cannot teach away from the use of bond wires because Farnworth's invention only pertains to improved pad forming processes. There is no prior art discussion concerning bond wires in Farnworth. Because Lee teaches positive reasons for using the bond wires in a chip package, it is proper to combine those teachings with Farnworth. Additionally, one of ordinary skill in the art understands that bond wires provide flexibility during the connection or electrical routing process. Bond wires can be easily attached or removed, lengthened or shortened to reach distant lead fingers and bond pads, or crossed over one another to form a desired electrical pathway. Such flexibility is beneficial for manufacturing a batch of chip packages having different

pathways or electrical functions. The trace connection of Farnworth has the disadvantage that once the conductive trace is connected to the active surface of the substrate it cannot be removed without a drastic change to the manufacturing process and the electrical pathways are physically limited as to how they can be connected across the span of the chip surface. Because the bond wires described by Lee provide flexibility during the connection process the manufacture of various types of semiconductor circuits possible. The discrete bond wires of Lee can be used with the conductive traces of Farnworth because Lee teaches well known benefits and the examiner has cited additional benefits. Both references disclose inventions involving semiconductor packages are analogous to each other and have been properly combined.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

MEW

August 25, 2003

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